REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended each of claims 6, 11 and 19 to recite that the Sn-Bi alloy layer is directly formed as a surface layer "before forming the soldered connection of the substrate and the semiconductor device". Similarly, claim 43 has been amended to recite that both of the electrodes are electrically connected with each other by means of a solder-containing portion, and wherein an Sn-Bi alloy layer is directly formed on the first electrode, as a surface layer, prior to forming the solder-containing portion, with this Sn-Bi alloy layer being in contact with a Pb-free solder, prior to forming the solder-containing portion, the solder-containing portion being made from the Pb-free solder. Furthermore, each of claims 78 and 83 has been amended to recite that the Sn-Bi alloy layer is formed directly on the lead, as a surface layer, prior to connecting the semiconductor device to the circuit board with the solder made of a Pb-free alloy.

Moreover, in order to simplify proceedings, claims 1-5, 24-27, 40-42, 50-61, 68, 69 and 72-77 have been cancelled without prejudice or disclaimer.

Applicants respectfully traverse the obviousness-type double patenting rejection as set forth in Item 6 on page 3 of the Office Action mailed December 31, 2002, in view of the following. Thus, this double patenting rejection is over the claims of copending Application No. 09/581,631. However, filed concurrently herewith is a Letter of Express Abandonment in Application No. 09/581,631, abandoning the application (No. 09/581,631). In view of the Letter of Express Abandonment submitted in Application No. 09/581,631, a copy of which is enclosed

herewith, it is respectfully submitted that the double patenting rejection in the above-identified application is moot.

It is respectfully submitted that abandonment of Application No. 09/581,631 does not constitute an admission as to the propriety of, or agreement with, the double patenting rejection; and does not constitute an admission as to the propriety of, or agreement with, arguments made by the Examiner in connection with the double patenting rejection. Abandonment of Application No. 09/581,631 does not constitute abandonment of the invention claimed therein, and it is respectfully submitted that abandonment of Application No. 09/581,631 facilitates and simplifies prosecution in connection with the above-identified application.

In view of the foregoing, and particularly in light of the concurrently filed Letter of Express Abandonment in Application No. 09/581,631, reconsideration and withdrawal of the rejection of all of the claims previously considered on the merits in the above-identified application, under the judicially created doctrine of obviousness-type double patenting over claims of Application No. 09/581,631, are respectfully requested.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the reference as applied by the Examiner in rejecting claims in the Office Action mailed December 31, 2002, that is, the teachings of U.S. Patent No. 6,110,608 to Tanimoto, et al., under the provisions of 35 USC §103.

It is respectfully submitted that the teachings of Tanimoto, et al. would have neither disclosed nor would have suggested such an electronic device as in the present claims, utilizing a Pb-free solder to connect a semiconductor device and a

substrate, and wherein a lead of the semiconductor device has an Sn-Bi alloy layer comprising 1-5 wt% Bi directly formed as a surface layer before forming the soldered connection of the substrate and the semiconductor device. See, e.g., claims 6, 11 and 19.

Furthermore, it is respectfully submitted that this applied reference would have neither taught nor would have suggested such an electronic device as in the present claims, having a first electrode provided on an electrical component electrically connected to a second electrode on a circuit board by a solder-containing portion, with an Sn-Bi alloy layer containing 1-5 wt% Bi directly formed on the first electrode, as a surface layer, and in contact with a Pb-free alloy, prior to forming the solder-containing portion, with the solder-containing portion being made from the Pb-free alloy. See claim 43.

Moreover, it is respectfully submitted that this applied reference would have neither taught nor would have suggested such an electronic device as in the present claims, having a semiconductor device connected to a circuit board via a solder made of a Pb-free alloy, the semiconductor device having an electrode structure which includes a lead and an Sn-Bi alloy layer containing 1-5 wt% Bi formed directly on the lead, prior to connecting the semiconductor device to the circuit board with the solder, the connection of the circuit board and the semiconductor being formed by soldering the Sn-Bi alloy and the solder (or wherein the connection is made by soldering during which the solder is initially in contact with the Sn-Bi alloy and melted, whereby the Sn-Bi alloy is melted and mixed with the solder). See claims 78 and 83.

In addition, it is respectfully submitted that the teachings of Tanimoto, et al. would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining claims, having features as discussed previously, and including (but not limited to) additional features such as including specific materials of the electrode as in, for example, claims 11, 19, 45 and 46; and/or wherein a copper layer is provided between the first electrode and the Sn-Bi alloy layer, as in, for example, claims 44, 53 and 82; and/or direct contact of the various structure as in claims 62-67.

Moreover, attention is respectfully directed to the enclosed Declaration of M. Okamoto. This Declaration, submitted under 37 CFR § 1.132, is being submitted for establishing the following:

(1) That the soldered connection formed using the Sn-Bi alloy layer containing about 1 to about 5 wt% Bi directly formed as a surface layer before forming the soldered connection of the substrate and the semiconductor device, as in the present invention, is a different structure than the layered structure in Tanimoto, et al., wherein initially two layers are formed and upon forming the soldered connection the two layers melt; and

(2) That the structure formed according to the present processing, wherein an Sn-Bi alloy layer comprising about 1-5 wt % Bi is directly formed as a surface layer before forming the soldered connection of the substrate and the semiconductor device, provides unexpectedly better results than the structure according to Tanimoto, et al.

In other words, it is respectfully submitted that the Declaration establishes that the presently recited processing forms a different product than that of Tanimoto, et al., and that this different product according to the present invention achieves unexpectedly better results, as discussed infra. It is respectfully submitted that particularly in view of the unexpectedly better results achieved according to the present invention as compared with the closest prior art structures, Applicants have established unobviousness of the presently claimed subject matter.

This evidence in the enclosed Declaration is in addition to advantageous effects achieved according to the present invention, as seen in Figs. 4-7 of Applicants' disclosure, showing advantages achieved by the present invention in strength and wettability. Such advantageous results as shown in Applicants' disclosure must be considered in a determination of unobviousness of the present invention. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984). Taking into account both the evidence in the enclosed Declaration and the evidence in Applicants' original disclosure, it is respectfully submitted that this evidence as a whole clearly establishes unobviousness of the presently claimed subject matter, rebutting any possible prima facie case of obviousness established by the teachings of Tanimoto, et al.

The present invention is directed to an electronic device having a soldered connection, for connection of the semiconductor device and the substrate. The present inventors directed their attention to the problem of reliability in providing the soldered connection, in the case where a lead-free solder is used for the connection; and, based on results of experimentation, have found that advantageous results in

the soldered connection are achieved when the bismuth content of a tin-bismuth alloy layer, on a lead connected by the solder, this layer being formed as a surface layer on the semiconductor device lead prior to forming the soldered connection, is 1-5 wt%.

That is, as described particularly on pages 5 and 6 of the specification of the above-identified application, a soldered connection of an electronic device, of a lead-free solder, is achievable using a tin-bismuth alloy layer having 1-5 wt% Bi on the lead, particularly when a tin-silver-bismuth alloy layer is used as the solder. Moreover, the soldered connection structure formed has high strength and a stable bond interface, and has good resistance to occurrence of whiskers. In addition, the tin-bismuth alloy layer with 1-5 wt% bismuth has good wettability. Thus, it is possible to obtain an interface having good bonding strength and wettability sufficient for practical use, and there is good resistance to formation of whiskers, so that it is possible to realize Pb-free electronic devices with a good, reliable and stable solder connection yet which are environmentally friendly.

Attention is respectfully directed to the enclosed Declaration under 37 CFR § 1.132 of M. Okamoto. This Declaration reports on the results of experimentation performed to investigate differences between (1) a soldered structure formed by plating only a single layer of Sn-Bi (having a thickness of 10 μm) on the lead of the semiconductor device prior to reflow-soldering, and (2) a soldered structure formed by plating two layers, of an alloy Sn-2Bi layer (having a thickness of 4 μm) and an inner Sn layer (having a thickness of 6 μm), on the lead of the semiconductor device prior to reflow-soldering. Note Item 13 bridging pages 3 and 4 of the enclosed Declaration. The specific experimental procedures performed in providing

specimens tested are set forth in Item 15 bridging pages 4 and 5 of the enclosed Declaration. Note that the comparative specimen corresponds to that disclosed in U.S. Patent No. 6,110,608 to Tanimoto, et al., having two layers; see Item 14 on page 4 of the enclosed Declaration.

Note that this Declaration investigated both the structure and state of fracture of the fractured surfaces of a lead side and a board side as observed by means of an electron microscope. See Item 17 on page 5 of the enclosed Declaration.

Attention is particularly directed to the four photographs shown in Fig. 1 of the enclosed Declaration, each of which shows a state of fracture of a surface of a solder joint. As set forth in Item 19 on page 6 of the enclosed Declaration, and as can be independently observed from the enclosed Fig. 1, the Bi phase is uniformly dispersed in the fracture surface of the solder joint (both on the lead side and on the substrate electrode side) formed using the lead structure with a single layer of Sn-1Bi (that is, the bismuth dispersion is homogeneous). In contrast, the Bi-phase is not uniformly dispersed in the fracture surface of the solder-joint (both on the lead side and on the substrate electrode side) formed using the lead structure with two layers, of Sn-2Bi layer and the Sn layer (that is, the bismuth dispersion is heterogeneous). See Item 19 on page 6 of the enclosed Declaration.

It is respectfully submitted that the Declaration clearly establishes that the structure formed by processing according to the present invention is different from structure formed according to processing as in Tanimoto, et al. Clearly this different structure, formed by the recited processing in the present claims, must be given weight in determining patentability. See In re Luck, 177 USPQ 523, 525 (CCPA 1973).

Attention is also directed to Items 20-22 on pages 6 and 7 of the enclosed Declaration. It is respectfully submitted that the analysis set forth therein clearly shows unexpectedly better results occurring with the structure according to the present invention. In this regard, note that in Item 20 it is stated that in solder joints, cracks or fracture (or separation) of a lead is liable to occur at an agglomeration site of Bi, so that it can easily be understood that the solder joint formed with utilization of a single Sn-Bi layer according to the present invention has a higher reliability in bonding than the solder joint formed using two layers as in Tanimoto, et al. Note also Item 21 on page 6 of the enclosed Declaration, setting forth the unexpectedly better stability achieved according to the present structure, because the Bi dispersion is homogeneous.

See the additional unexpectedly better results achieved by the present invention as set forth in Item 23 of this Declaration. Therein, it is stated that a single plating process for a single plating layer, for leads of semiconductor devices, as in the present invention, is advantageous as compared with double plating processes for two plating layers, as in Tanimoto, et al., in the view point of saving of production cost and improvement of productivity.

As can be seen in the foregoing, the structure according to the present invention is different from, and unexpectedly better than, the structure formed in Tanimoto, et al., for example, in having better (more homogeneous) dispersion of bismuth; and provides unexpectedly better results. This evidence, by itself, clearly establishes unobviousness of the presently claimed invention; and, as indicated previously, particularly in light of the evidence in Applicants' original disclosure as

seen in Figs. 4-7 thereof, establishes unobviousness of the presently claimed subject matter.

Tanimoto, et al. discloses a lead material for an electronic part, a lead and a semiconductor device using the same. The lead material is one in which the surface of a conductive substrate is coated with a plated layer made of a tin group,material which does not contain Pb, so that the lead material does not give an adverse influence to the environment because it does not contain Pb, and it also has excellent solderability (or solder wettability) and provides a strong junction with a solder, and does not cause non-uniform thickness of the plated layer even in reflow processing. The described structure has a lead material with a first plated layer and a second plated layer provided on a surface of a conductive substrate in this order, a melting temperature of the material of the second plated layer being lower than that of a material of the first plated layer. See column 2, lines 43-49. This patent discloses that the lead material for the electronic part can include a first plated layer made of a Sn substance and a second plated layer made of a Sn alloy containing at least one element selected from a group of Ag, Bi, Cu, In and Zn; or, alternatively, the first plated layer can be made of a Sn alloy containing at least one element selected from a group of Ag, Cu, Sb and Y and a second plated layer made of a Sn substance. See column 2, lines 50-60. As to the Sn-Bi alloy, this patent discloses that the Bi percentage content can be up to 87 wt%. See column 4, lines 23-27. However, this patent further discloses that if the lead material provides a junction with a solder and 20 wt% or more Bi exists at the solder part, the junction strength of the solder part gradually deteriorates, so that the alloy composition is preferably adjusted such that the Bi percentage content at the junction part after soldering is

20 wt% or less. This patent further discloses that an Sn-Bi alloy having a Bi content of 30 wt% or less as the Sn alloy is generally preferred. See column 4, lines 48-62.

Tanimoto, et al. is directed to a problem when a single plating layer of a lead-free material is formed on a conductive substrate, taking into account the environment, and in order to solve this problem, proposes to provide a lead material in which a first lead-free plating layer and a second plating layer are formed on the substrate, the melting temperature of the second plating layer being lower than that of the first lead-free plating layer. It is respectfully submitted that the disclosure of Tanimoto, et al. would have neither taught nor would have suggested the lead-free solder for the connection, particularly using the specific tin-bismuth alloy as the alloy layer with the lead-free solder as in the present claims, and advantages achieved thereby. That is, it is emphasized that Tanimoto, et al. is silent with respect to use of a Pb-free solder, disclosing the lead material having the first and second plated layers yet without disclosure of a Pb-free solder.

It is emphasized that the lead material of Tanimoto, et al. has a conductive substrate with first and second plating layers in sequence on the substrate. It is respectfully submitted that the second plating layer has a lower melting point than that of the first plating layer, so that the first plating layer serves as a barrier layer for preventing diffusion of copper from the conductive substrate during soldering (note, for example, column 3, lines 44-47 of Tanimoto, et al.).

However, it is respectfully submitted that the lead material of Tanimoto, et al. has the following problems. The bonding strength is low because an insufficient amount of intermetallic compound is formed between the first plating layer (which is not melted) and the conductive substrate. Furthermore, in a case where the first

plating layer has a different chemical composition from the second plating layer, or where the first plating layer is different from the second plating layer in bismuth content, there arises a problem of non-uniform chemical composition in a bonding solder after the reflow-soldering process, as can be seen in the enclosed Declaration; and, thereafter, during use of a semiconductor device with a lead material as in Tanimoto, et al., there will occur diffusion between the first plating layer and the solder so as to alleviate the non-uniformity of the chemical composition, resulting in that the connecting structure changes gradually in chemical composition, so that stability and reliability of the connection changes. In addition, in the case of the first plating layer of tin being provided on the second plating layer of tin-bismuth, there also arises a problem of occurrence of whiskers. In addition, and as can be appreciated from the manufacturing process, by use of the two plating layers the number of production process steps is increased and production cost also increases.

In contrast, according to the present invention utilizing the tin-bismuth alloy layer with relatively small amount of bismuth, formed as a surface layer directly on the lead, with the Pb-free solder, the foregoing problems in connection with use of the two plating layers can be avoided.

In addition, attention is also directed to those of the present claims which further include a copper layer between the lead substrate and the tin-bismuth layer. An advantage of this structure, which has an intermediate layer of copper, is described on pages 13-15 of Applicants' specification. It is respectfully submitted that Tanimoto, et al. does not disclose, nor would have suggested, the presently claimed

subject matter including the copper layer, or advantages thereof as in the present invention.

The contention by the Examiner in Item 9 on page 4 of the Office Action mailed December 31, 2002, that Tanimoto, et al. specifically discloses that his invention also covers embodiments where the two-layer structure plated layers are melted, and the components such as Bi or Ag, contained in a new plated layer formed during re-solidifying after melting, are in the state of dilution by Sn. However, as shown by the enclosed Declaration, the structure wherein the two plated layers are melted, forms a different structure than that of the present invention, in, for example, homogeneous dispersion of bismuth; and, moreover, the present structure formed using a layer as deposited has unexpectedly better results. Particularly in view thereof, it is respectfully submitted that Tanimoto, et al. would have neither taught nor would have suggested the presently claimed invention.

Contentions by the Examiner in Item 11 bridging pages 5 and 6 of the Office Action mailed December 31, 2002, are noted. The fact remains that Tanimoto, et al. specifically and expressly discloses use of a Pb-containing solder, in testing used in examples in this patent. Note particularly column 7, lines 52-57, disclosing a molten eutectic solder. Of course, use of the double layer structure of Tanimoto, et al., even with a Pb-containing solder, could limit use of Pb by avoiding Pb in a layer between the lead and solder. In any event, it is respectfully submitted that Tanimoto, et al. would not have disclosed, nor would have suggested, a Pb-free solder as in the present claims and as discussed previously, especially in light of the testing using an eutectic solder.

The further contention by the Examiner in the first three lines on page 6 of the Office Action mailed December 31, 2002, that it is clear from Tanimoto, et al. that this reference clearly understands that Pb-containing alloys should not be used "and that they have been replaced by lead free alloys in current practice", is noted. The Examiner has provided no evidence supporting this contention, with respect to structure in Tanimoto, et al. It is respectfully submitted that such contention is shown to be incorrect in light of use of eutectic solder (that is, Pb-containing solder) in the testing procedure in the examples described in Tanimoto, et al.

In view of the foregoing comments and amendments, and particularly in light of the enclosed Declaration, reconsideration and allowance of all claims remaining in the application are respectfully requested.

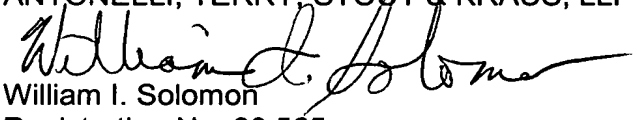
Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The changes are shown on the Attachment captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135

(Case No. 500.38665CX1) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

6. (Twice Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder, the semiconductor device having a lead on which an Sn-Bi alloy plating layer comprising 1 to 5 wt% Bi is directly formed as a surface layer before forming the soldered connection of the substrate and the semiconductor device.

11. (Twice Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder, the semiconductor device having a lead made of Cu or a Cu alloy on which an Sn-Bi alloy layer comprising about 1 to about 5 wt% Bi is directly formed as a surface layer before forming the soldered connection of the substrate and the semiconductor device.

19. (Twice Amended) An electronic device comprising a substrate and a semiconductor device, which are connected with each other by means of a Pb-free solder, the semiconductor device having a lead made of an Fe-Ni alloy on which an Sn-Bi alloy plating layer comprising 1 to 5 wt% Bi is directly formed as a surface layer before forming the soldered connection of the substrate and the semiconductor device.

43. (Amended) An electronic device which comprises a first electrode provided on an electronic component and a second electrode formed on a circuit

board, the both electrodes being electrically connected with each other by means of a [solder] solder-containing portion, wherein an Sn-Bi alloy layer containing 1 to 5 wt% Bi is directly formed on the first electrode, as a surface layer, prior to forming the solder-containing portion, and the Sn-Bi alloy layer is in contact with a Pb-free solder, prior to forming the solder-containing portion, the [solder, which is] solder-containing portion being made [of a] from the Pb-free solder [alloy, and the solder is in contact with the second electrode].

78. (Amended) An electronic device comprising:

a semiconductor device having an electrode structure which comprises a lead and a Sn-Bi alloy layer containing 1-5 wt% Bi which is formed directly on the lead; and

a circuit board which is connected to the semiconductor device with a solder which is made of Pb-free alloy,

wherein the Sn-Bi alloy layer is formed directly on the lead prior to connecting the semiconductor device to the circuit board with said solder, and

wherein the connection is formed by contacting and soldering the Sn-Bi alloy layer and the solder.

83. (Amended) An electronic device comprising:

a semiconductor device having an electrode structure which comprises a lead and a Sn-Bi alloy layer containing 1-5 wt% Bi which is formed directly on the lead; and

a circuit board which is connected to the semiconductor device with a solder which is made of a Pb-free alloy,

wherein the Sn-Bi alloy layer is formed directly on the lead prior to connecting the semiconductor device to the circuit board with said solder, and

wherein the connection is formed by soldering during which the solder is initially in contact with the Sn-Bi alloy and subsequently melted, whereby the Sn-Bi is melted and mixed with the solder under heat from the solder.